Process Introduction

1.5um BiCMOS Process Technology

Process features

- P substrate and P-epi
- Twin well
- LOCOS
- High performance bipolar devices
- Dual gate oxide available（optional）
- Low voltage CMOS(5V)
- High voltage CMOS(30V)
- High poly resistor(optional)
- Double metal

Key Design Rules

14 Masks	Min. Width/Space(um)
Active	1.5/3
PBASE	3.0
Poly	1.5/2
Cont	1.5
M1	2/2
Via	2
M2	3/3

Device Specification

Device	Parameter	Specification			
		Min	Typ	Max	Unit
NPN（Ae=5x7um2）	Hfe(Ic=100uA)		100		-
	BVceo(Ic=10uA)	12	-	-	V
Substrate-PNP（Ae=10x10um2）	Hfe(Ic=10uA)		110		-
	BVceo(Ic=10uA)	12	-	-	V
LPNP (Wb=4um)	Hfe(Ic=10uA)		40		-
	BVceo(Ic=10uA)	12	-	-	V
LV-NMOS (W/L=20/1.5)	Vth(Vds=0.1V)		0.7		V
	BVdss		12		V
LV-PMOS (W/L=20/1.5)	Vth(Vds=0.1V)		-0.8		V
	BVdss		12		V
HV-NMOS (W/L=50/3)	Vth(Vds=0.1V)		1.2		V
	BVdss	30			V
HV-PMOS (W/L=50/3)	Vth(Vds=0.1V)		-1.3		V
	BVdss			-30	V
Sheet Resistance	PBASE-R(20x200um^2)	-	2.5k	-	Ω/□
	Poly-R(20x200um^2)	-	23	-	Ω/□
	High Poly-R		2.0		kΩ/□
	NWell-R		1.2		kΩ/□
Capacitance	Gate capacitance		1.75		fF/um2
	Capacitance(Poly/DN)	-	1.05	-	fF/um2